Claim 1 stands rejected under 35 U.S.C. § 102 as being anticipated by Sedra et al., Mizutani ('418), Burr et al. ('912) and JP '888. Solely to expedite prosecution, claim 1 has been canceled rendering the rejections thereto moot.

Claim 2 is the sole independent claim currently rejected over prior art.

Claim 2 stands rejected under 35 U.S.C. § 102 as being anticipated by Mizutani ('418), Kaya et al. ('384), Burr et al. ('912) and JP '888. This rejection is respectfully traversed for the following reasons.

As a preliminary matter, it is noted that the Examiner has not provided Applicants a copy of relied on USP No. 5,780,912 to Burr et al. nor has he made it of record. Instead, the Examiner provided and cited USP No. 5,650,340 to Burr et al. which was not relied on by the Examiner in the pending rejection. For purposes of this response and in order to expedite prosecution, Applicants have relied on Burr et al. ('340) as a basis for response to the pending rejection. It is respectfully requested that the Examiner provide and make of record Burr et al. ('912) in the next Office Action. Furthermore, if any subsequent rejection is issued which relies on either Burr et al. patent ('340 or '912), it is respectfully requested that such an Office Action be made non-final to give Applicants a fair chance to fully review and respond to the Examiner's specific reliance on the particular Burr et al. patent relied on.

Claim 2 recites in pertinent part, "a channel region is formed near the surface of said semiconductor region directly above said embedded drain region such that the channel region reaches the surface of said semiconductor region." It is respectfully submitted that none of the cited prior art disclose or suggest the aforementioned feature in combination with the other features recited in claim 2.

As shown in Fig. 1A of Applicants' drawings, the top of the embedded drain region 17a does not reach the substrate surface in the channel region 11a of the semiconductor substrate 11. As a result, as shown in Fig.1B, due to the spread of the depletion layer made by the voltage applied to the drain region 17 and the voltage applied to the control gate electrode 15, the isoelectric lines 20 bend in the direction parallel to the substrate near the substrate surface. The carriers (electrons) running near the substrate surface in the channel region lla are placed in an electric field having an element perpendicular to the substrate, driven by the bent isoelectric lines 20. The electrons are subject to an external force having an upward element perpendicular to the substrate, as shown by the arrow in Fig. 1B. Since the floating gate electrode 13 is formed in the direction of the arrow, the electron injection efficiency can be increased.

Turning to the relied on portions of Mizutani, the Examiner alleges that it "is understood that a channel is formed near the surface of the semiconductor region above the embedded drain region." However, Mizutani (Fig. 6) discloses only a drain region 20 formed above the embedded drain region 21 which reaches the substrate surface. Mizutani is completely silent as to a channel region formed directly above the embedded drain. Accordingly, Mizutani does not disclose or suggest, *inter alia*, "a channel region ... directly above said embedded drain region" as recited in claim 2.

Turning to the relied on portions of Kaya et al., the Examiner again alleges that it "is understood that a channel is formed near the surface of the semiconductor region above the embedded drain region." However, similar to Mizutani, Kaya et al. (Fig. 10e) discloses an embedded drain region 20 completely buried in a drain region 12, whereby only the drain region 12 is formed above the embedded drain region 20 so as to reach the substrate

surface. Kaya et al. is completely silent as to a channel region formed directly above the embedded drain. Accordingly, Kaya et al. does not disclose or suggest, *inter alia*, "a channel region ... directly above said embedded drain region" as recited in claim 2.

Turning to the relied on portions of Burr et al., the Examiner again alleges that it "is understood that a channel is formed near the surface of the semiconductor region above the embedded drain region." Burr et al. (Fig. 3) discloses an embedded doped region 47' which can be formed on the drain side. However, depending on which side the region 47' is formed, only the corresponding source or drain region is formed above the region 47' so as to reach the substrate surface. Burr et al. (Fig.3) is completely silent as to a channel region formed directly above the region 47'. Accordingly, Burr et al. (Fig. 3) does not disclose or suggest, *inter alia*, "a channel region ... directly above said embedded drain region" as recited in claim 2.

Turning to the relied on portions of JP '888, the Examiner again alleges that it "is understood that a channel is formed near the surface of the semiconductor region above the embedded drain region." However, JP '888 (Fig. 14) discloses only an embedded drain region 12b with drain region 6b,8b,11b formed directly thereabove which reaches the substrate surface. Accordingly, JP '888 does not disclose or suggest, *inter alia*, "a channel region ... directly above said embedded drain region such that the channel region reaches the surface of said semiconductor region" as recited in claim 2.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "**inherency may not be established by probabilities or possibilities**" (*see Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)) in a single prior art reference, Akzo N.V. v. U.S. Int'l Trade

Commission, 808 F.2d 1471 (Fed. Cir. 1986), and because none of Mizutani ('418), Kaya et al. ('384), Burr et al. ('912) and JP '888 disclose or suggest the combination of features recited in claim 2, it is submitted that Mizutani ('418), Kaya et al. ('384), Burr et al. ('912) and JP '888 do not anticipate claim 2, nor any claims dependent thereon. In addition, it is submitted that claims 3-12 are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on all the foregoing, it is submitted that claims 2-12 are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection of claims 2-12 under 35 U.S.C. § 102 be withdrawn.

CONCLUSION

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

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APPENDIX

IN THE SPECIFICATION

The paragraph beginning on page 2, line 7 has been amended as follows:

--Further, for higher probability of carrier injection, high voltage must be applied to the control gate electrode 205 for raising the potential bias between the floating gate and the drain, in order to electrically pull hot electrons toward the floating gate [304] electrode 203.--

The paragraph beginning on page 74, line 7 has been amended as follows:

--First, referring to FIG. 27A, a protective oxide film 21 made of silicon oxide is formed on the main surface of the semiconductor substrate 11, for example, made of silicon (Si), to protect the surface of the semiconductor substrate 11, by the thermal oxidation method, CVD method or other techniques. Subsequently, boron (B) ions are injected into the semiconductor substrate 11, which is the p-type impurity for controlling the threshold voltage, at an injection energy of about 30keV and a [doze] dose of 5.0 x $10^{12}/cm^2$ - 1.0 x $10^{13}/cm^2$.--

IN THE CLAIMS

2. (Amended) A nonvolatile semiconductor memory device comprising:

a floating gate electrode formed on a semiconductor region via a first dielectric film;

a control gate electrode capacitively coupled with said floating gate electrode via a second dielectric film; and

a source region and a drain region that are formed in said semiconductor region on side regions of said floating gate electrode and control gate electrode;

wherein the end of said drain region faced with said source region has an embedded drain region extending toward said source region without reaching the surface of said semiconductor region, and

a channel region is formed near the surface of said semiconductor region directly above said embedded drain region [in] such that the channel region reaches the surface of said semiconductor region.

3. (Amended) The nonvolatile semiconductor memory device according to claim 2, further comprising an embedded region adjacent an upper area that is formed in an upper part of said embedded drain region in the semiconductor region and has a conduction type opposite to that of said drain region.

4. (Amended) The nonvolatile semiconductor memory device according to claim 3, wherein an impurity concentration in said embedded region [adjacent upper area] is higher than that in said semiconductor region.

5. (Amended) The nonvolatile semiconductor memory device according to claim 3, wherein said embedded drain region has a conduction type opposite to that of said drain region and an impurity concentration lower than that in said embedded region [adjacent upper area].

6. (Amended) The nonvolatile semiconductor memory device according to claim 2, wherein said embedded drain region has the same conduction type as that of said drain region [and an impurity concentration lower than that in said drain region].

7. (Amended) The nonvolatile semiconductor memory device according to claim 2, further comprising an embedded region adjacent a lower area that is formed in the lower part of said embedded drain region in said semiconductor region and has a conduction type opposite to that of said drain region.

8. (Amended) The nonvolatile semiconductor memory device according to claim 7, wherein an impurity concentration in said embedded region [adjacent lower area] is higher than that in said semiconductor region.